India

Overweight *(no change)*

Highlighted Companies

Cyient DLM Ltd

ADD, TP Rs880, Rs659 close

Cyient DLM offers electronics solutions for mission-critical applications with high entry barriers in regulated sectors like aerospace & defence, medical technology and industrials. The company has built a healthy client base in the past with a strong parentage. We currently have an ADD rating on the stock.

Kaynes Technology

ADD, TP Rs2800, Rs2424 close

Kaynes Technology focuses on low-volume, high-mix business with specialized product offerings for higher margins. The proportion of higher value-added services has increased over the past few quarters. We have an ADD rating on the stock.

Syrma SGS Technology

ADD, TP Rs660, Rs568 close

Syrma has a strong EMS portfolio, which has moved towards the consumer segment. It aims for strategic acquisitions to increase scale, market share and new products, and expects to improve wallet share, geographic reach, and client base. We have an ADD rating on the stock.

Summary Valuation Metrics

P/E (x)	Mar24-F	Mar25-F	Mar26-F
Cyient DLM Ltd	76.76	46.35	31.39
Kaynes Technology	75.57	57.54	40.61
Syrma SGS Technology	67.73	44.24	30.62

P/BV (x)	Mar24-F	Mar25-F	Mar26-F
Cyient DLM Ltd	5.41	4.84	4.2
Kaynes Technology	12.3	10.14	8.11
Syrma SGS Technology	5.95	5.24	4.48

Dividend Yield	Mar24-F	Mar25-F	Mar26-F
Cyient DLM Ltd	0%	0%	0%
Kaynes Technology	0%	0%	0%
Syrma SGS Technology	0%	0%	0%

EMS

OSAT: India to replicate Malaysian way

- OSAT is the back-end process in making semiconductors which involves chip packaging. Access to cheap labour & utilities acts as a key differentiator.
- Malaysian OSAT companies enjoy the highest EBITDA margin in this space, even higher than the market leaders, due to lower cost of manufacturing.
- We feel India has all the ingredients - right from PLI incentives to power subsidy - to succeed. Sustained push from the government is key in the near term.

Automobile sector to drive the next phase of OSAT business growth

The OSAT industry was previously dominated by mobile/communication device manufacturers. However, the communication market appears to be saturated, with OSATs having major exposure to this segment showing tepid growth. What is interesting to note is that semiconductor/OSAT companies having high exposure to the automobile sector are posting good QoQ numbers. A case in point is that of Infineon Tech, one of the largest automobile chip manufacturers. Amkor, the second-largest OSAT, is also showing good growth, compared to the market leader ASE, which is lagging due to its mobile/PC sector exposure. Advanced driving assistance (ADAS) and autonomous vehicle segments are driving this growth, with these segments expected to post a 20-25% CAGR over the next five years. Kaynes Technology also has a significant exposure to the PCB requirements of the automotive sector (~38% in FY23), and hence, presents an interesting optionality for the company as and when its OSAT division matures.

OSAT business to be margin-accretive for Kaynes Technology

Kaynes Technology has partnered with Globetronics, a Malaysian OSAT company, for technology transfer. The Malaysian OSAT industry is unique, in the sense that it tends to make higher EBITDA margin (~35%) vs. even market leaders like ASE/Amkor (~20%). In the OSAT space, companies generally tend to compete on lower labour costs coupled with access to cheaper utilities. Malaysian companies have access to cheapest electricity & water rates in Asia and rest of the world. In fact, power costs form around 8-10% of their revenue in the OSAT space. This, coupled with lower labor costs compared to Taiwan, makes Malaysian companies margin leaders in this space. We feel India has similar characteristics, which will help the OSAT industry to succeed. Hyderabad provides electricity at Rs7.7/kwh, marginally higher than the electricity rate in Penang (Rs6.4/kwh). Moreover, labour costs in India are cheaper compared to Malaysia, suggesting that Kaynes Technology will be able to improve its current EBITDA margin profile of 14-15%.

Kaynes Technology's OSAT plant to generate lucrative RoCE

Kaynes Technology to invest Rs28.5bn in its Telangana plant, out of which Rs7.12bn will be borne by the state government via incentives and Rs14.3bn will be met by the central government. Hence, the company will be investing only Rs7.13bn in the said project. We expect it to generate an asset turn ratio of 0.4-0.6x at peak capacity utilization, while attaining an EBITDA margin of 14-15%. This will result in RoCE generation of 20% at the lower band, which, we believe, is quite healthy.

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Figure 1: Lucrative RoCE likely from Kaynes Technology's OSAT capex powered by government incentives

EBITDA Margin/Asset Turns	0.2	0.4	0.6	0.8	1
10%	3%	11%	19%	27%	35%
11%	4%	13%	21%	30%	39%
12%	5%	14%	24%	33%	43%
13%	5%	16%	26%	37%	47%
14%	6%	17%	29%	40%	51%
15%	7%	19%	31%	43%	55%

SOURCES: INCRED RESEARCH, COMPANY REPORTS

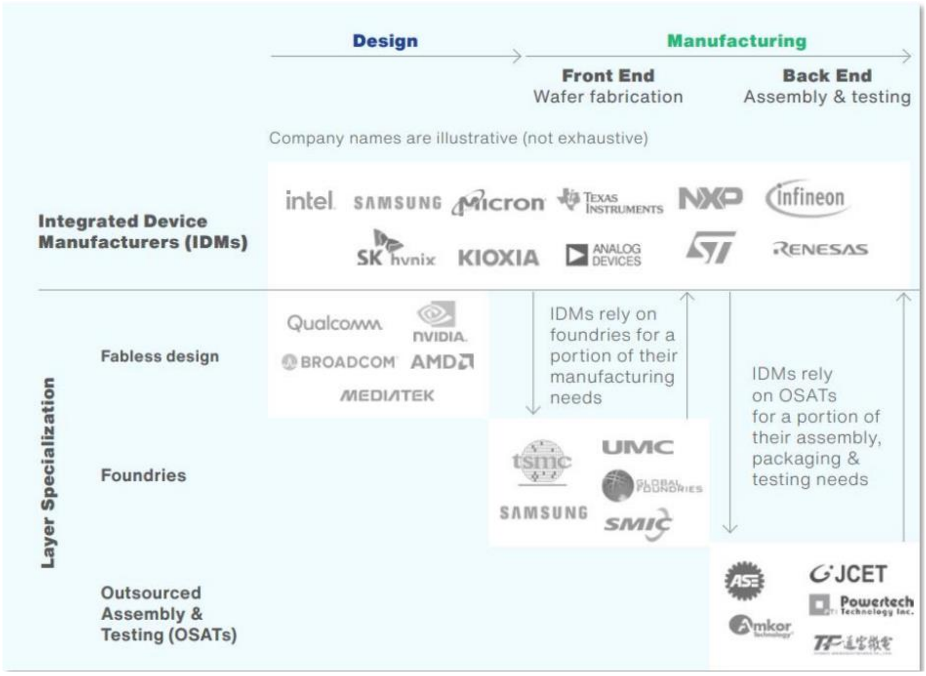
What is OSAT?

Outsourced Semiconductor and Testing (OSAT) players have an extremely important role in the semiconductor industry, as they are the bridge that covers the gap between semiconductor foundries and end-consumers. OSAT companies are contracted by semiconductor design companies, such as Intel, AMD and Nvidia and are told to execute based on their designs. Intel, for instance, outsources its chip packaging to various OSATs for assembly and test services before they ship the chip to its customers. As of 2020-end, the OSAT market was valued at US$31.6bn and is expected to touch US$49.7bn, growing at a CAGR of 7.3% over the next five-to-six years. The increased demand from the automotive sector and IoT (Internet of Things)-connected devices are viewed as the main driving force in the foreseeable period.

Before moving ahead, let's look at the entire value chain

The entire semiconductor value chain consists of integrated device manufacturers (IDM), fabless design, foundries and OSAT.

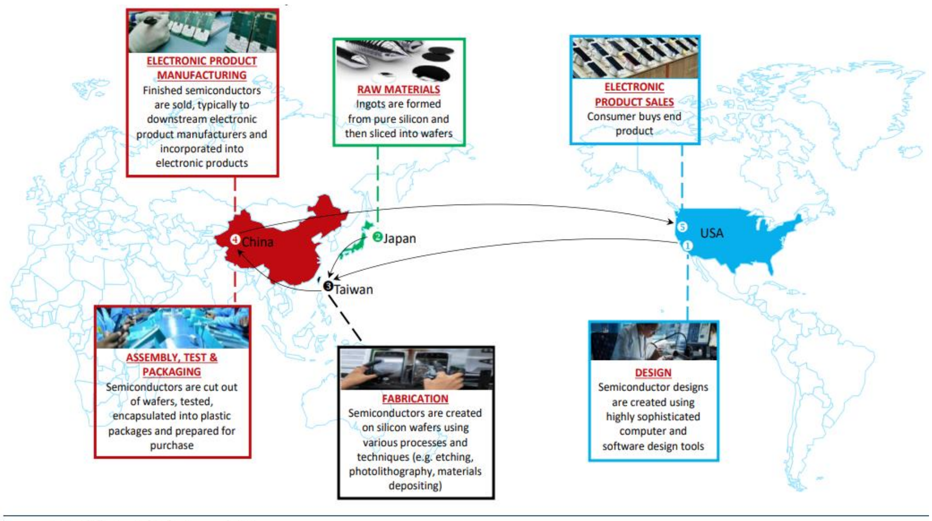
Figure 2: Micron and Kaynes Technology to set up plants in India mainly for meeting the OSAT part of the supply chain



SOURCE: INCRED RESEARCH, COMPANY REPORTS

How the supply chain is spread out globally ➤

Figure 3: China/Taiwan hold a major share in OSAT market

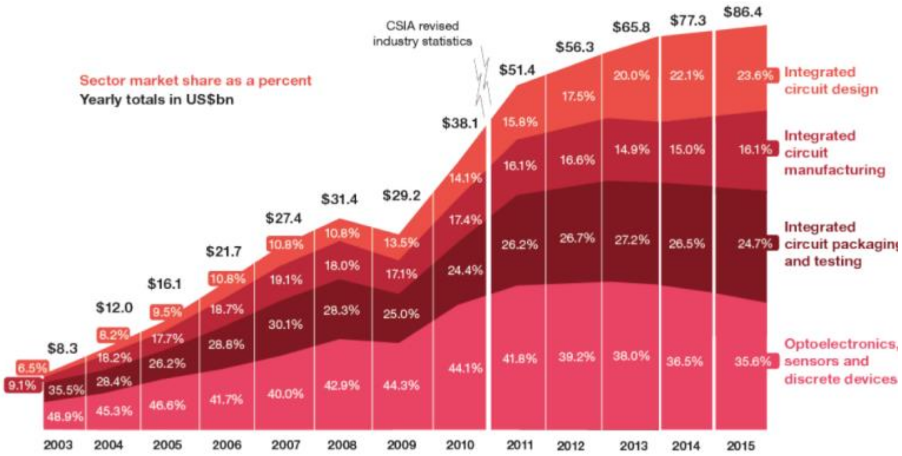


SOURCE: INCRED RESEARCH, COMPANY REPORTS

China's OSAT market ➤

At the end of 2015, China had 123 OSAT facilities in operation, representing 22% of the total number of worldwide OSAT facilities and 34% of worldwide OSAT manufacturing floor space (a proxy for potential manufacturing capacity). As a result, these facilities ranked first – in both the number of facilities and share of OSAT manufacturing floor space. This was noticeably ahead of Taiwan (with 93 facilities for just more than 21% of worldwide OSAT space) and Japan (113 facilities for 9% of OSAT space).

Figure 4: China's OSAT industry by sector

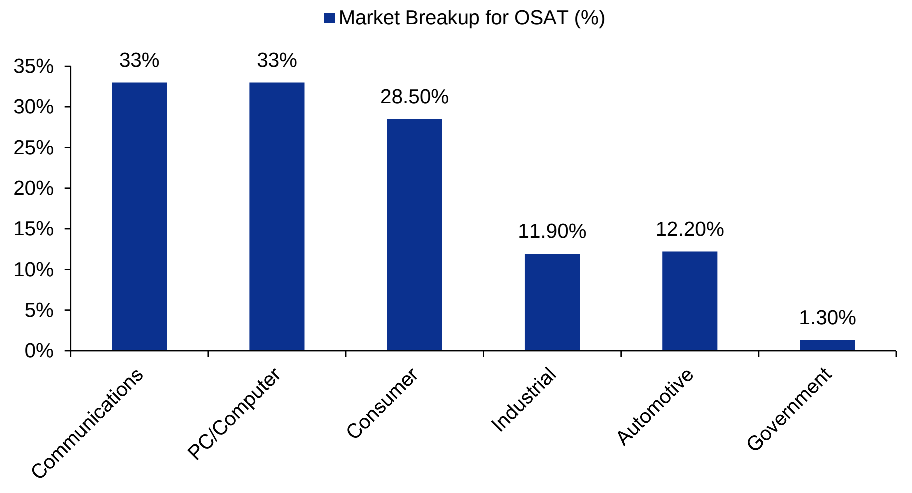


SOURCE: INCRED RESEARCH, COMPANY REPORTS

OSAT market by industry ➤

The smartphone segment has been the biggest source of revenue for OSAT providers, with more than 1bn shipments every year. Recently, the market has become saturated and is declining. With the macroeconomic headwinds prevailing in the US leading to decreased consumer spending, it has resulted in companies in this segment posting a weak set of numbers.

Figure 5: OSAT market by end-industry



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Automobile industry to drive the next phase of OSAT growth

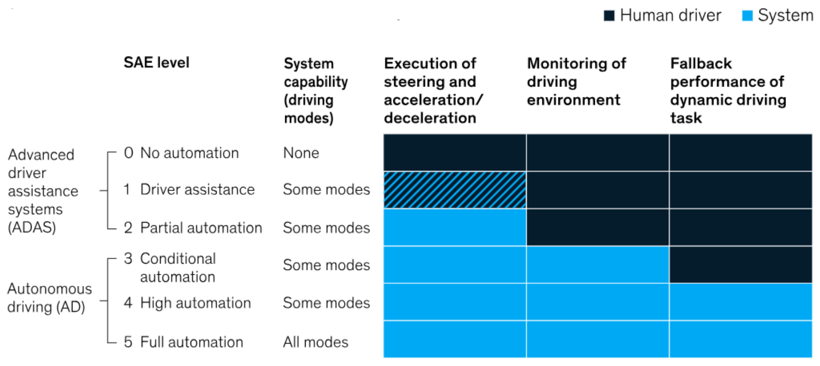
The growing popularity of electric vehicles and driverless vehicles have called for semiconductor technology advancements in the automotive industry, the ones that would make the space smarter and energy efficient. The applications of semiconductor chips in the automotive space are in the following areas:

- **Improved connectivity:** As drivers, we have become acquainted with using features like route mapping and road closure using in-vehicle GPS – features that run by the integration of semiconductor technology in cars. High-grade legacy node semiconductors fine-tune preinstalled systems in the vehicle. The semiconductor is also used to process and sense key data of the vehicle's computing system, leading to reliable, accurate, and timely control of the vehicle.
- **Advanced driving assistance:** One of the key selling points of autonomous driving vehicles is their braking system which works in a fraction of seconds - an area where the benefits of semiconductor technology in automobiles are most visible. The software powers features such as cruise control, emergency braking system, blind-spot detection systems, parking camera assist, collision-avoiding sensors, etc. in a way that they respond in real time.
- **Autonomous vehicles:** One of the biggest revolutions of the current times has been autonomous vehicles. These vehicles can move from one point to another without any human assistance in an 'autopilot mode' through the help of artificial intelligence or AI-based technology. To fine tune this heavily sophisticated model, advanced semiconductors are being used by the automotive industry.

Advanced driving assistance (ADA) is driving huge demand

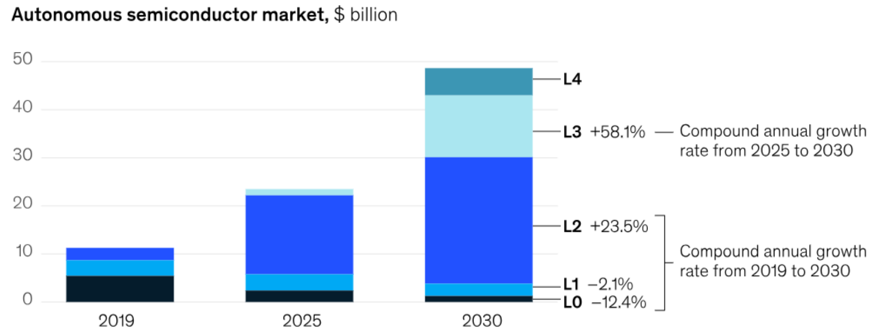
Vehicles in levels 0 through 2 (entry) achieve adequate performance with standard chips, but those in levels 2 (advanced) through 5 are expected to require a growing share of specialty silicon. Such chips are more efficient, enable rapid performance increases within vehicle systems, and allow the execution of complex software functionalities and analytics, such as those that enable sensor fusion of cameras, laser, LiDAR, and other devices. Many auto OEMs have started designing chips in-house and hence, are outsourcing the testing and packaging part to global OSAT companies.

Figure 6: Autonomous vehicles have been divided into levels based on their capabilities, as per SAE (Society for Automotive Engineers)



SOURCE: INCRED RESEARCH, COMPANY REPORTS

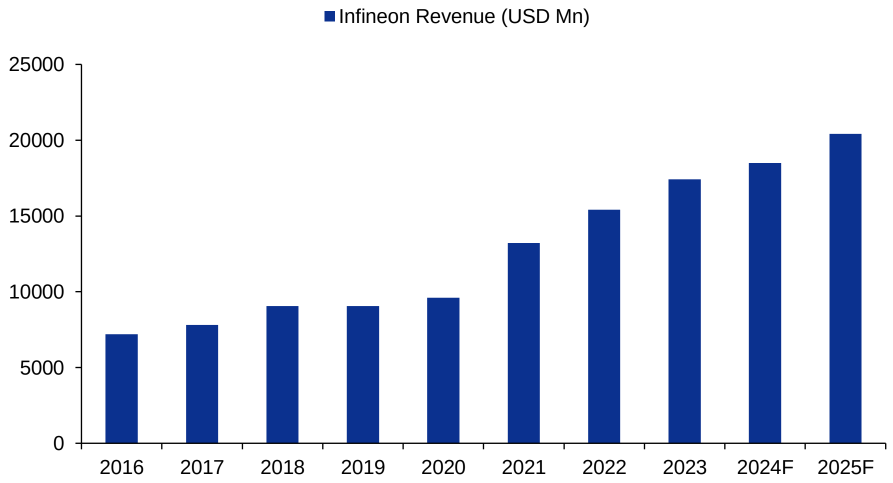
Figure 7: Complex SAE level i.e., L2 and L3, to post highest CAGR in the coming years



SOURCE: INCRED RESEARCH, COMPANY REPORTS

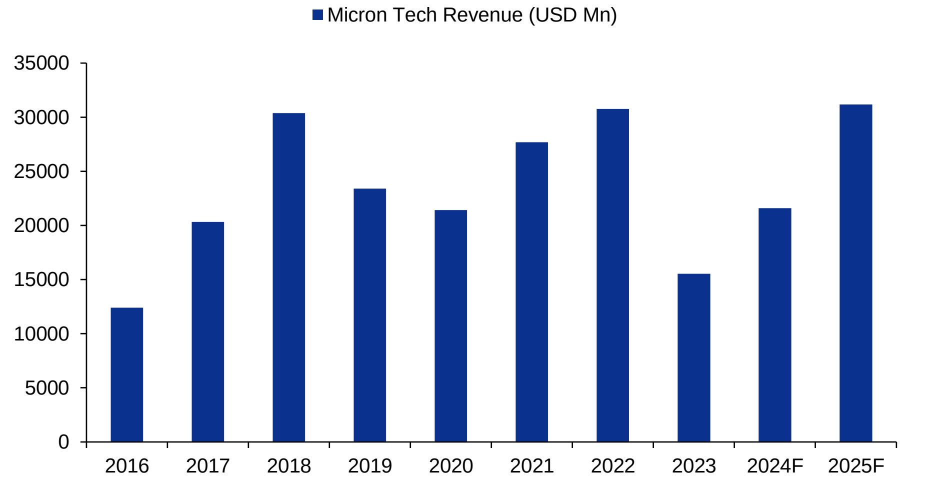
Automobile semiconductors are posting good growth when there is a downturn in the consumer space like phones/computers

Figure 8: Infineon, one of the largest automotive chip IDMs, has posted huge growth in its topline in FY22; consensus estimates also factor in the huge growth



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 9: On the other hand, Micron Technologies, which mainly deals with consumer electronics (memory devices) is facing serious headwinds



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Players in global OSAT market

The OSAT market is a consolidated market, with the top 10 players combined having an 84% market share. Chinese and Taiwanese players dominate this space. The prospects for Kaynes Technology, which is entering this space via a technological partnership with Globetronics, a Malaysian OSAT player, will be discussed later in this report.

Figure 10: Revenue figures for top 10 OSAT players

Rank 2020	Rank 2019	Company	Area	Revenue 2019 (US$ m)	Revenue 2020 (US$ m)	Annual growth %	Market share in 2019	Market share in 2020
1	1	ASE	Taiwan, China	8352.144	7823.232	10.91%	30.50%	30.11%
2	2	Amkor	US	4009.824	4497.984	12.17%	14.64%	14.62%
3	3	JCET	China Mainland	3091.104	3681.072	19.09%	11.29%	11.96%
4	4	PTI	Taiwan, China	2192.112	2517.552	14.85%	8.01%	8.18%
5	5	TFME	China Mainland	1190.88	1553.616	30.46%	4.35%	5.05%
6	6	HUATIAN	China Mainland	1167.12	1209.6	3.64%	4.26%	3.93%
7	7	KYEC	Taiwan, China	840.096	957.024	13.92%	3.07%	3.11%
8	9	Chip MOS	Taiwan, China	675.648	760.464	12.55%	2.47%	2.47%
9	10	Chipbond	Taiwan, China	673.2	736.128	9.35%	2.46%	2.39%
10	8	UTAC	Singapore	700.416	662.4	-5.43%	2.56%	2.15%
Top 10 - total				**22,893**	**25,839**	**12.87%**	**83.60%**	**83.98%**
Other				**4,490**	**4,929**	**9.77%**	**16.40%**	**16.02%**
Total				**27,383**	**30,768**	**12.36%**	**100.00%**	**100.00%**

SOURCE: INCRED RESEARCH, COMPANY REPORTS

ASE vs. Amkor - leaders in OSAT space

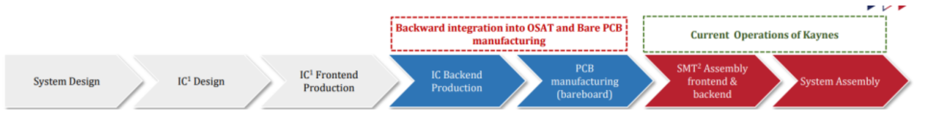
ASE and Amkor are the two largest OSAT companies in the world, with a combined 56% global sales market share. They both provide packaging and testing for leading IDMs and fabless chipmakers. Both companies also have exposure to a wide range of end-markets such as communications, automotive and computing devices. These companies not only stand to benefit from the development of 5G, AI and HPC technologies leading to increased chip complexity and demand, but the industry is also boosted by the trend of semiconductor companies outsourcing their packaging, testing and manufacturing requirements as they increasingly rely on independent providers of packaging and testing and electronic manufacturing services (EMS). As market leaders, ASE and Amkor are well positioned to benefit from these trends. However, there are several distinct features of these companies. To cite an example, in terms of business structure, ASE has a larger scale and a more diversified business along the value chain with its EMS business segment. Based in Taiwan, ASE also enjoys closer proximity to the highly active manufacturing Asian-Pacific region by having a strategic alliance with the world's largest fab TSMC (TSM). Nonetheless, Amkor is a global player with significant scale and has expanded after the strategic acquisition of JDevices, Japan's largest fab, to advance its automotive market growth strategy while ASE is counting on 5G business, with Qualcomm (QCOM) as a key partner. **As**

mentioned earlier in the report, due to high growth in the automotive OSAT space, it presents Amkor a unique opportunity due to its higher revenue exposure to the automotive division.

Kaynes Technology is following the ASE model

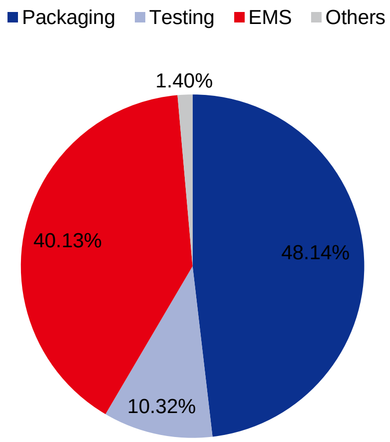
Between ASE and Amkor, ASE has a more diversified business, with complementary services providing electronic manufacturing services while Amkor provides only assembly and testing services. This makes ASE the one-stop shop for semiconductor companies to meet their packaging, testing and EMS needs. EMS refers to the process of value-added manufacturing and testing services involving electronic components, which follows the OSAT process in the value chain. Thus, it is more convenient for its customers as the company can fulfill all its needs along the value chain. This complementary relationship is one of the factors behind the company achieving its scale advantage, with EMS accounting for 40% of its revenue. The company's EMS business is also highly complementary with its largest end-market, communications, which is also the largest contributor to its EMS revenue, at 45%.

Figure 11: OSAT is backward integration to PCB assembly - the current business model of Indian EMS players



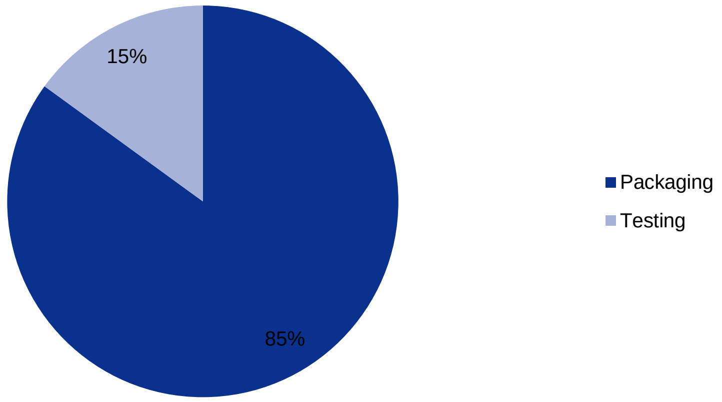
SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 12: ASE Industries' revenue breakup



SOURCE: INCRED RESEARCH, COMPANY REPORTS

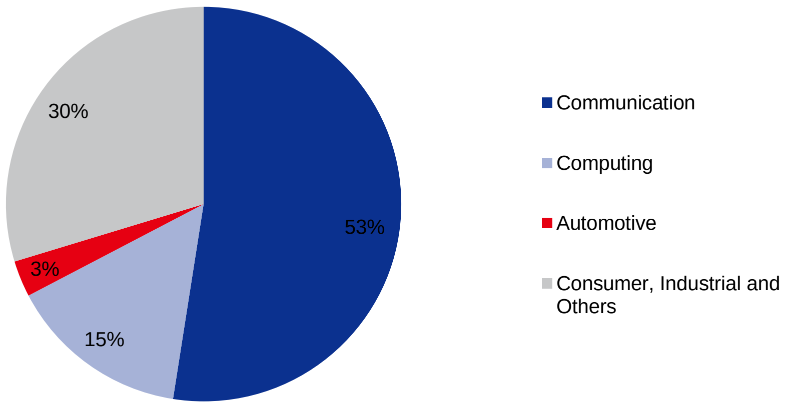
Figure 13: Amkor's revenue breakup



SOURCE: INCRED RESEARCH, COMPANY REPORTS

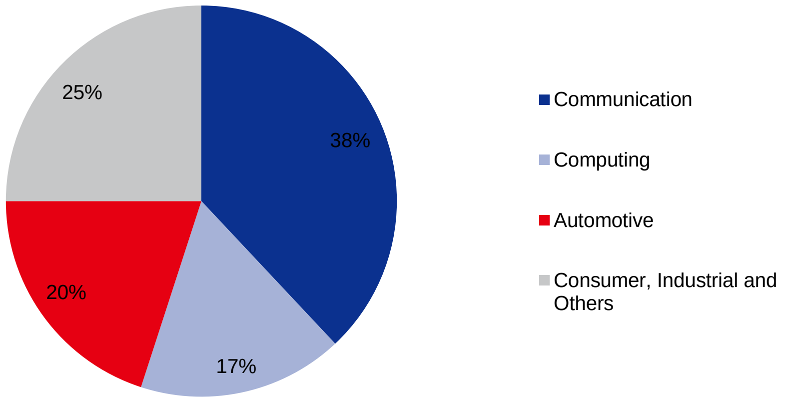
Amkor leads the high-growth automotive market while ASE focuses on communications market

Figure 14: Revenue breakup by end-clients for ASE Group



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 15: Revenue breakup by-end clients for Amkor Group



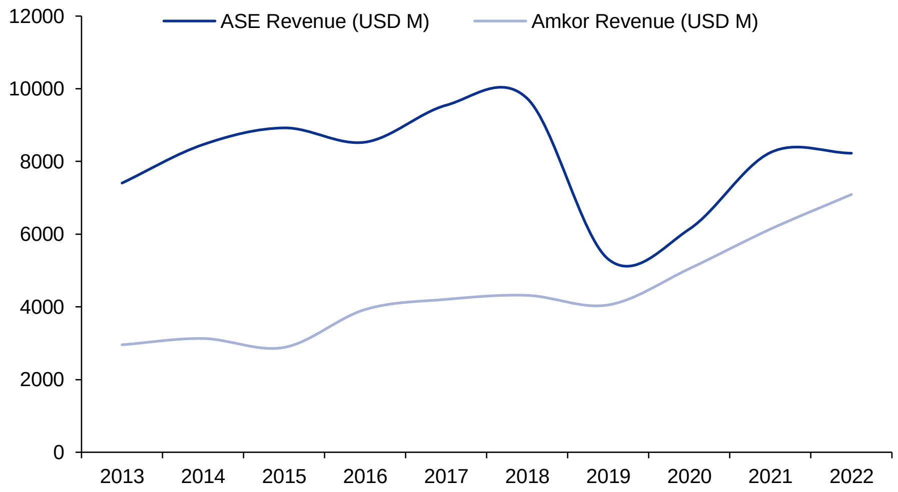
SOURCE: INCRED RESEARCH, COMPANY REPORTS

Strategic alliance between ASE and TSMC

ASE, based in Taiwan, is one of the leading centres for outsourced semiconductor and electronics manufacturing in the world. Its close geographical proximity allows the company to benefit from strong manufacturing activity. The company has maintained a strategic alliance with TSMC since 1997, the largest dedicated foundry with a market share of 56% of foundry market revenue. The alliance has made ASE the preferred provider of packaging and testing services for TSMC clients. This allows ASE to benefit from leveraging TSMC's clients comprising leading companies such as Apple, Qualcomm, Nvidia, MediaTek and NXP Semiconductors, who account for nearly half of ASE's revenue. Apple, Qualcomm and MediaTek are major players in the smartphone processor market and are developing 5G chipsets that require advanced packaging capabilities which ASE can provide. Given the long-standing relationship between TSMC and ASE, the alliance between these companies is expected to continue as it enables them to provide a total semiconductor manufacturing solution along with close geographic advantage for both market leaders. This means that ASE should be able to continue counting on TSMC's clients comprising leading chipmakers.

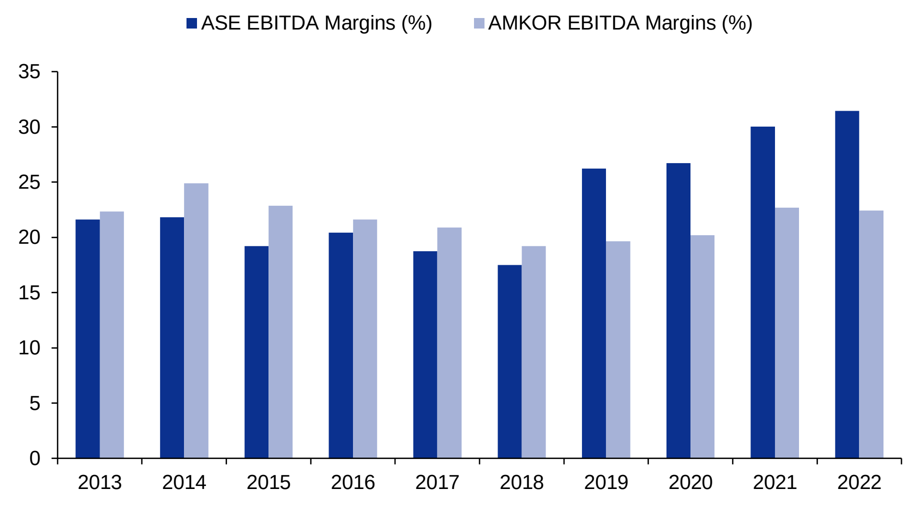
Financial analysis of ASE and Amkor

Figure 16: ASE is facing headwinds due to its exposure to consumer electronics companies; meanwhile Amkor, due to its automotive space exposure, is showing growth



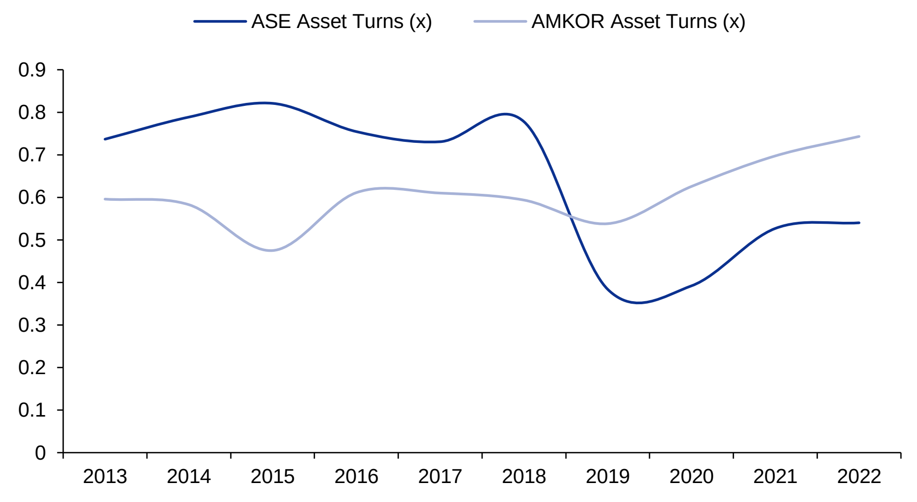
SOURCES: INCRED RESEARCH, COMPANY REPORTS

Figure 17: Both companies enjoy EBITDA margin in the range of 20-25%



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 18: 0.5x-0.7x would be an ideal range in respect of asset turn ratio for these companies



SOURCE: INCRED RESEARCH, COMPANY REPORTS

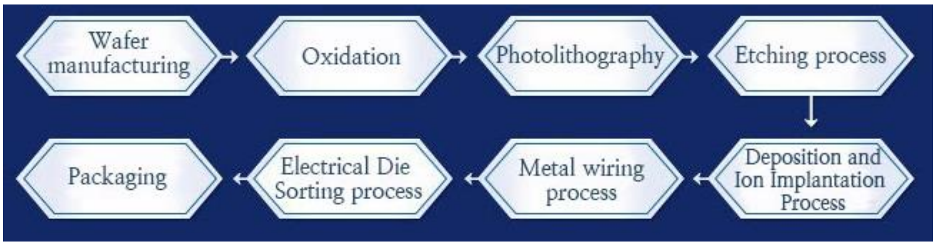
The eight-step process of manufacturing semiconductors

- **Wafer manufacturing:** The main raw material for making semiconductors is silicon. For silicon to turn into a semiconductor chip, it needs to go through eight processes, the first of which is wafer manufacturing. Semiconductors are stacked high and solid to form a complex structure like a high-rise building. Constructing a building starts with a foundation. A wafer is the foundation for semiconductors. Most wafers are made of silicon extracted from sand. First, sand is heated until it melts into a high purity liquid and then it is solidified by crystallization. The resultant silicon rods are called ingots. These ingots are sliced into a disc called wafers. The surface of the sliced wafer is rough and contains defects, and so polishing machines are used to polish the surface of a wafer. The reason is that defects on the surface could negatively affect the precision of circuits. If you look at the surface of wafer, you will see a biscuit pattern on the surface. This is because the word wafer comes from biscuit wafers. Because the larger the diameter, the greater the number of chips that can be produced per wafer. So, the diameter of wafers is becoming larger. As the resultant thin disc-shaped wafer is not conductive yet, a process to make wafers semi-conductive is required.
- **Oxidation:** Wafers, then go through the oxidation process, in which oxygen or water vapour is sprayed on the water surface to form a uniform oxide film. This

oxide film protects the wafer surface and protects current leakage between circuits.

- **Photolithography:** Just as you draw blueprints to build a building, you draw a circuit design onto a wafer, which is called the photolithography process. It is also called 'photo' in short, as it is like developing a photo taken from a film camera. With semiconductors, a photomask functions as the film. A photomask is a glass substrate with a computer-designed circuit pattern. To draw the circuit on the wafer, photoresist, a material that responds to light, is applied thinly and evenly on the oxide film previously placed on the wafer. Now, when light transfers the patterned photomask, the circuit is drawn on the wafer surface. After an inspection on the wafer, to check whether the pattern is drawn well, we move onto the next step.
- **Etching:** Now, unnecessary materials are carved out so that only the designed pattern remains. Using a liquid or gas etchant, unnecessary materials are selectively removed, to draw the desired design.
- **Deposition and ion implantation:** Let's imagine constructing a building on a semiconductor chip, smaller than a fingernail and thinner than a sheet of paper. The photolithography process and the etching process are repeated several times on the wafer, layer by layer. Here an insulating film, that separates the layers, is required. It is called a thin film. Coating a thin film at a desired molecular level on a wafer is called deposition. As the coating is so thin, precise and sophisticated technology is required to uniformly apply the thin film on a wafer. To give this semiconductor electrical characteristics, ion implantation is also required. A semiconductor made of silicon doesn't conduct electricity, but by adding impurities it conducts current. Hence, after all these processes, the wafer becomes conductive and numerous circuits are drawn on it.
- **Metal wiring & EDS:** It is the process of testing electrical characteristics to make sure that each individual chip has achieved the desired quality level. In other words, it is a testing step to sort out defective chips. **Yield is the number of working chips relative to the maximum chip count on a single wafer.** The semiconductor chips selected through the EDS process are made in a form suitable for devices.
- **Packaging: The last and most important step, from an Indian perspective**. This is the step where Micron Tech, Kaynes Technology, CG Power and others will be operating. The wafer completed through the previous process is cut into individual semiconductor chips that can be loaded on an electronic device. An individual chip must have a path to exchange electrical signals with the outside world and have a form to protect it from various external elements. The wafer is cut into individual chips and the diced or sawed chips are placed on the printed circuit board or PCB. In the bonding step, the contact point of the semiconductor chip placed on a substrate is connected with the contact point of the substrate. Finally, moulding finishes the chip package to its desired shape.

Figure 19: The eight steps of manufacturing semiconductors at a glance

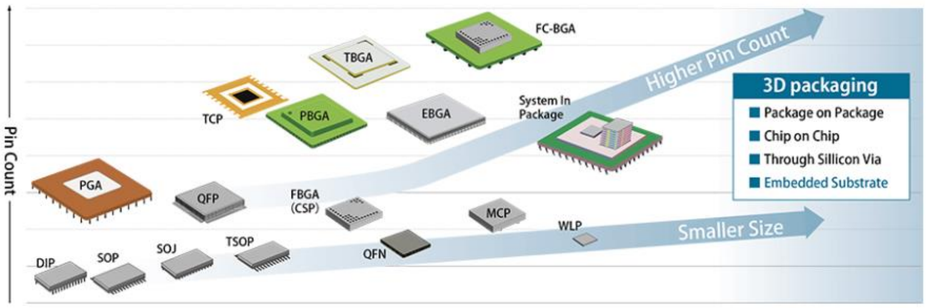


SOURCE: INCRED RESEARCH, COMPANY REPORTS

Delving deeper into semiconductor packaging ›

Semiconductor packaging materials play an important role in protecting the integrated circuit or IC chips from the surrounding environment, ensuring electrical connection for the chip mounted on printed circuit boards or PCBs. High-speed, high integration and low power consumption ICs accompanying the rapid progress of electronics technology such as AI, cloud computing, intelligentization of automobiles, and also miniaturization and thinning of electronic devices typified by smart phone and wearable devices have led to the demand for semiconductor packages fulfilling the high density, multilayer and low-profile requirements. **Semiconductor packages require three characteristics: 1) Smaller packaging with high density. 2) High pin-count for high integration with multiple functions. 3) High heat dissipation characteristics and high electric properties enabling high performance.**

Figure 20: Classification of different packaging methodologies

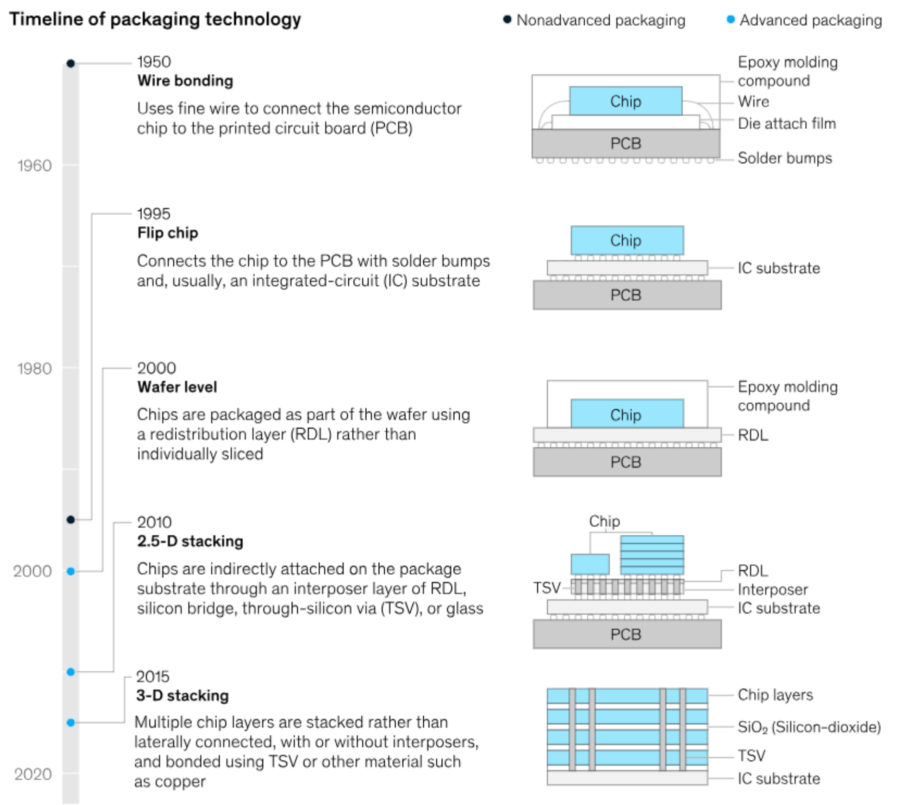


SOURCE: INCRED RESEARCH, COMPANY REPORTS

Timeline of various packaging methodologies ›

Kaynes Technology will be operating in the non-advanced semiconductor packaging space.

Figure 21: Evolution of various semiconductor packaging methodologies



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Traditional packaging techniques ›

Developed in the 1950s and still in use today, wire-bond technology is an interconnection technique that attaches the printed circuit board (PCB) to the die - the silicon square that contains the integrated circuit - using solder balls and thin metal wires. It requires less space than packaged chips and can connect relatively distant points, but it can fail in high temperatures, high humidity, and temperature cycling, and each bond must be formed sequentially, which adds to the complexity and can slow down manufacturing. The wire-bonding market is likely to be valued at about US$16bn by 2031F, with a CAGR of 2.9 percent, according to Mckinsey.

The first major evolution in packaging technology came in the mid-1990s with flip chips, which use a face-down die, the entire surface area of which is used for interconnection through solder 'bumps' that bond the PCB with the die. This results in a smaller form factor, or hardware size, and a higher signal-propagation rate - that is, faster movement of signals from the transmitter to the receiver. Flip-chip packaging is the most common and lowest-cost technology currently in use, mainly for central processing units, smartphones, and radio-frequency system-in-package solutions. Flip chips allow for smaller assembly and can handle higher temperatures, but they must be mounted on very flat surfaces and are not easy to replace. The current flip-chip market is valued at around US$27bn, with a projected CAGR of 6.3 percent, which should bring it to US$45bn by 2030F, according to Mckinsey.

Wafer-level packaging/advanced packaging ›

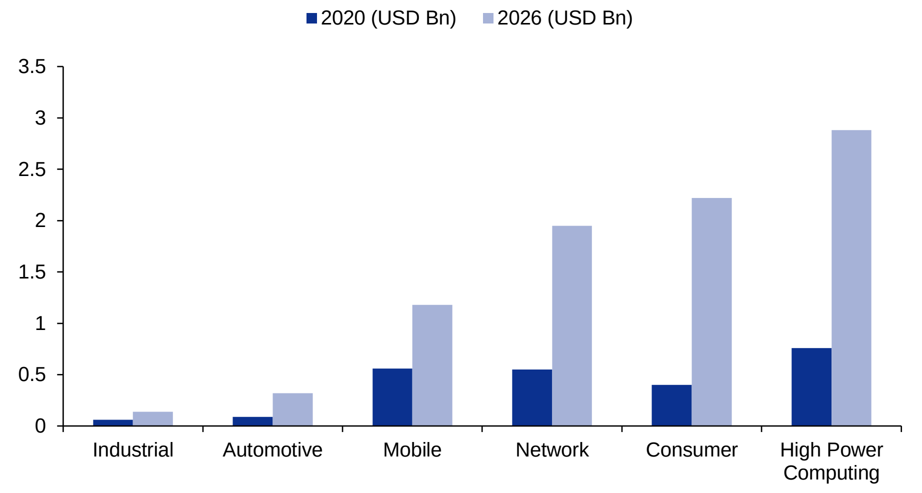
As the benefits of Moore's law reach their limits, advances in chip performance rely more on the back-end of production, including packaging. While traditional packaging 'dices' the silicon wafer into individual chips first and then attaches the chips to the PCB and builds the electrical connections, wafer-level packaging makes the electrical connections and moulding at the wafer level, and then dices the chips using a laser. The greatest difference between wafer-level chip-scale packaging (WLCSP) and flip chips, in terms of chip configuration, is that WLCSPs have no substrate between the die and the PCB. Instead, redistribution layers (RDLs) replace the substrate, leading to a smaller package and enhanced thermal conduction.

Wafer-level packaging is divided into two types: fan-in and fan-out. In fan-in wafer-level packaging, used mainly for low-end mobile phones that require rudimentary technology, the RDLs are routed toward the centre of the die. In the fan-out version, which was introduced in 2007, the RDL and solder balls exceed the size of the die, and so the chip can have more inputs and outputs while maintaining a thin profile. Fan-out packaging comes in three types: core, high density, and ultra-high density. Core, which is used mostly for automotive and network applications that don't require high-end technology - such as radio frequency and infotainment chips - accounts for less than 20 percent of the almost US$1.5bn fan-out packaging market. High and ultra-high density are mostly used for mobile applications and are expected to expand to some network and high-performance computing applications. The world's largest maker of WLCSPs is the Taiwan Semiconductor Manufacturing Company (TSMC).

Growth in advanced packaging market ›

The advanced packaging market is driven by the end-application of various technologies. Since the mid-2010s, fan-out wafer-level packaging has dominated, with about 60 percent of the market share. Fan-out packaging is cheaper than stacking and is engineered for high heat resistance and a small form factor. These attributes make it appropriate for mobile applications, which are likely to generate most of its demand, followed by the automotive space.

Figure 22: Advanced packaging market is expected to post good growth



SOURCES: INCRED RESEARCH, COMPANY REPORTS

Apple uses fan-out advanced packaging for its application processors, graphic chips, and 5G and 6G modem chips. It is the largest user of the technology, consuming most of the volume produced by TSMC. Other top fabless players - that is, companies that design and sell hardware and chips but outsource their manufacture - are also using fan-out technology in mass-produced chips. Most of the growth in HPC and network applications is likely to come from AI chips, edge computing, and network chips in consumer devices, which require the small form factor and affordable costs that fan-out packaging can offer.

Kaynes Technology's entry into OSAT powered by government incentives

Kaynes Technology is foraying into the field of OSAT with a Rs28,500m investment in Telangana. Out of this Rs 28,500m, Rs7,125m will be borne by the state government via incentives and Rs14,250m will be borne by the central government. Hence, Kaynes Technology will be only investing Rs7,125m in the said project. We expect the company to generate an asset turn ratio of 0.4-0.6 while running at peak capacity while attaining an EBITDA margin of 14-15%. This is based on the rationale that Kaynes Technology is entering non-advanced packaging, where companies generally compete based on costs and have no such technological differentiation.

Figure 23: RoCE generation for Kaynes Technology's OSAT plant at different financial metrics

EBITDA Margin/Asset Turns	0.2	0.4	0.6	0.8	1
10%	3%	11%	19%	27%	35%
11%	4%	13%	21%	30%	39%
12%	5%	14%	24%	33%	43%
13%	5%	16%	26%	37%	47%
14%	6%	17%	29%	40%	51%
15%	7%	19%	31%	43%	55%

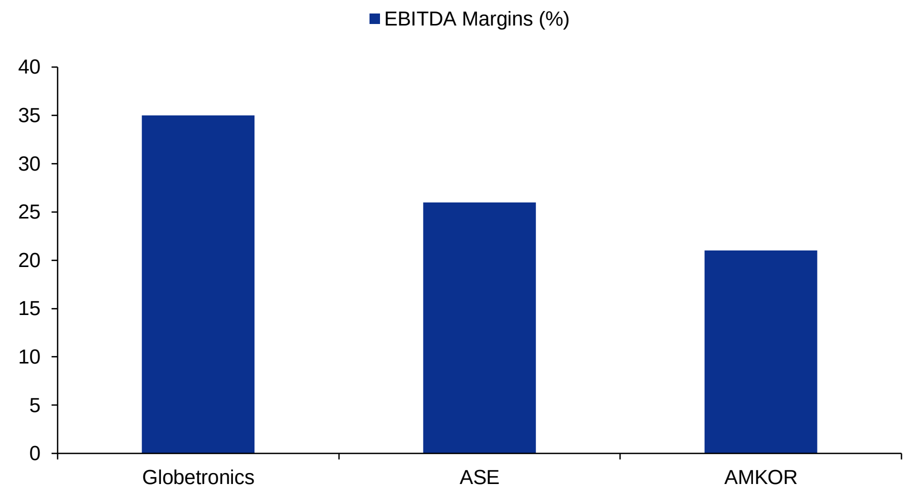
SOURCE: INCRED RESEARCH, COMPANY REPORTS

Kaynes Technology's partnership with Globetronics, a Malaysian OSAT player

Kaynes has chosen Globetronics as its technology partner for its foray into the OSAT Industry. Globetronics is a Malaysian OSAT company, mainly into making the sensors for phones (the company derives 60% of its revenue from this division). The remaining topline is generated from OSAT of smart LED headlamps used in automobiles and OSAT of quartz time-keeping devices. However, the quartz timekeeping devices OSAT is low-margin business for the company and hence, it is slowly phasing it out. A brief look at the financials of the company shows that Globetronics enjoys around 30% EBITDA margin in the OSAT space. This is because Malaysia has one of the cheapest utilities (electricity and water) rates in Asia and the rest of the world. This gives Globetronics a cost advantage over foreign peers.

Globetronics has better EBITDA margin than ASE/Amkor

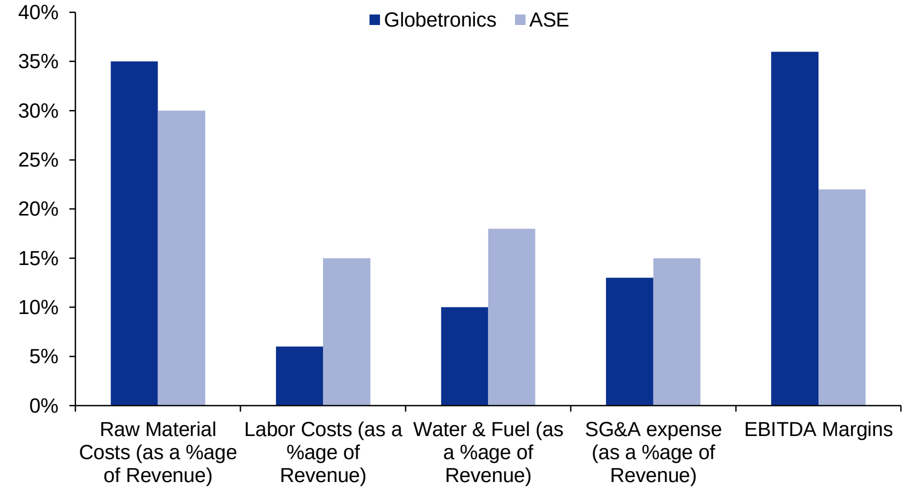
Figure 24: Higher margin for Globetronics is because of cheaper utilities & labour costs



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Malaysian OSAT companies have access to cheaper utilities

Figure 25: Malaysian companies have cheaper labour and power costs compared to OSAT peers in other countries

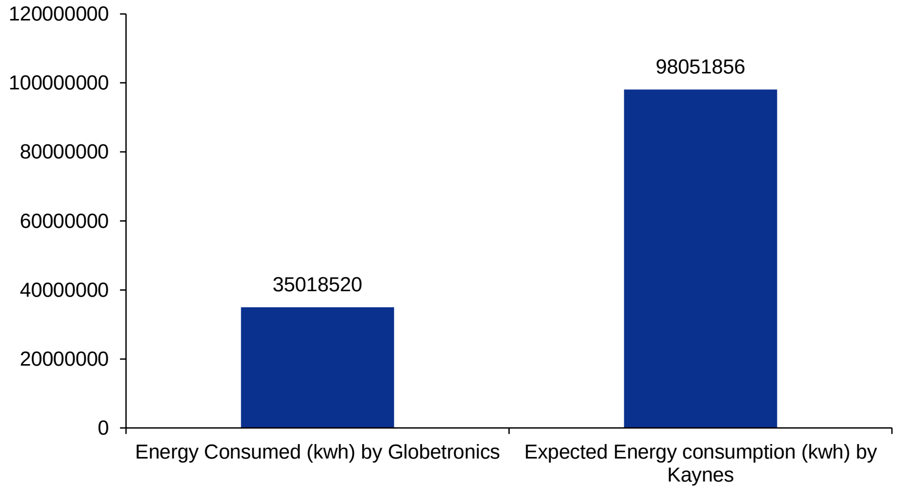


SOURCE: INCRED RESEARCH, COMPANY REPORTS

Comparison of cost of utilities in India and Malaysia

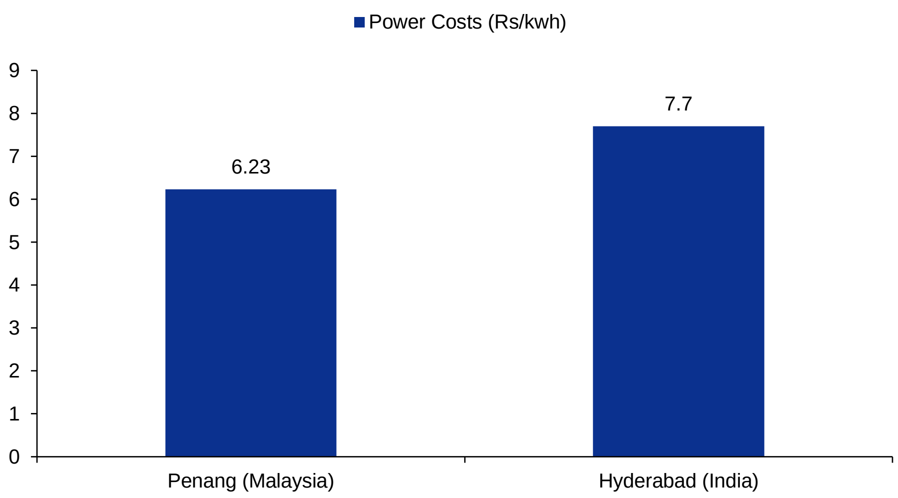
Kaynes Technology has opted for setting up an OSAT plant in Telangana, which provides lucrative subsidies on power costs, making India cost-competitive with Malaysia. Power costs form roughly 8-10% of the total topline for Globetronics. **Power cost in Hyderabad is 24% more expensive than Penang, which will result in a 250-350 bp lesser EBITDA margin for Indian OSAT companies.**

Figure 26: This chart assumes that Kaynes Technolgy's plant area is 2.8x that of Globetronics



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 27: Power tariff for industries is subsidized in Hyderabad but still it's ~24% more expensive than what it is in Penang

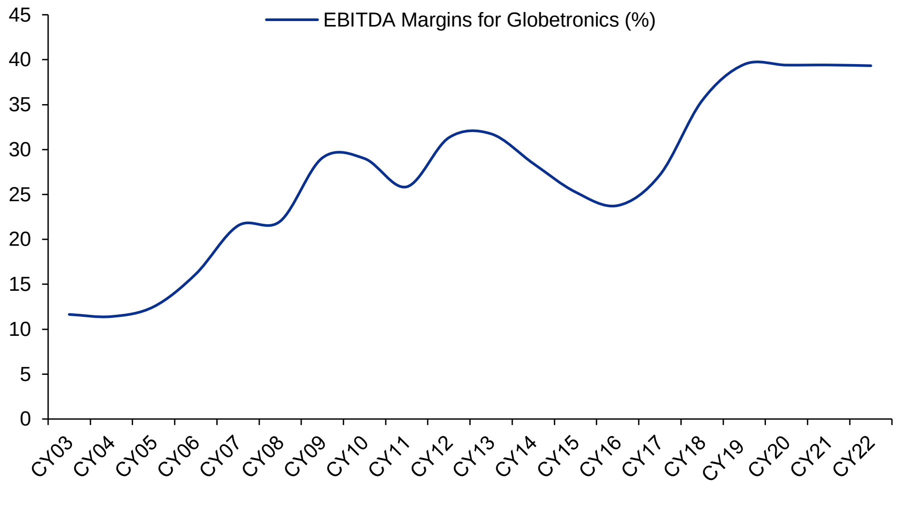


SOURCE: INCRED RESEARCH, COMPANY REPORTS

OSAT to be margin-accretive for Kaynes Technology

Kaynes Technology will initially perform OSAT in wire-bonding in BGAs, and gradually move up the value chain with flip chip and wafer chip packaging. Given that utilities and labour costs in India are cost-competitive with Malaysia, we expect Kaynes Technology to maintain its current EBITDA margin profile, and even improve it as the asset utilization rate goes up. However, the presence of a semiconductor ecosystem in the country will also aid in further margin expansion, as was seen in the case of Globetronics.

Figure 28: Improvement in the semiconductor ecosystem leads to an improvement in margins for Globetronics

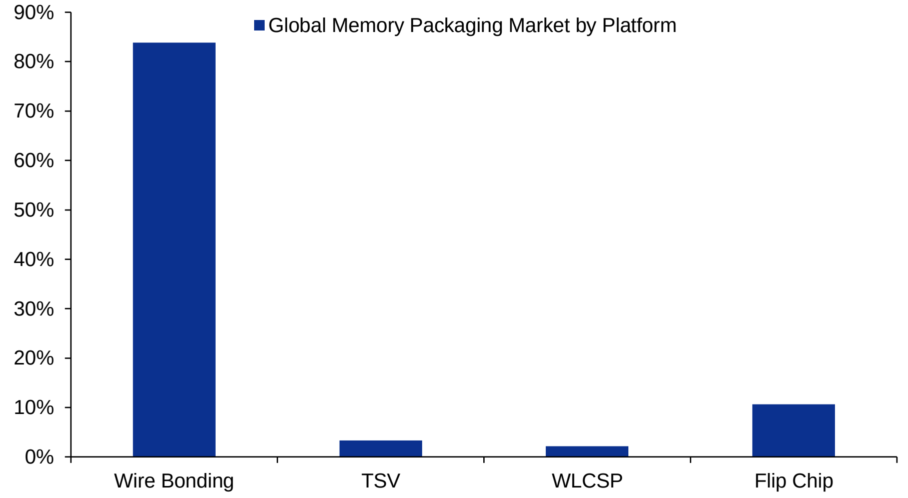


SOURCE: INCRED RESEARCH, COMPANY REPORTS

The other entrant into OSAT space: Micron Technologies (Not Rated)

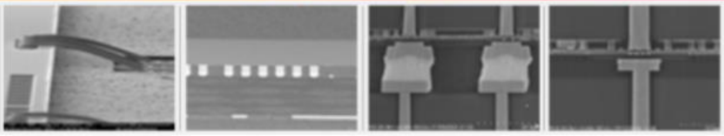
Micron Technologies will be venturing into the OSAT business by setting up a plant at Sanand in Gujarat. This is important as Micron Technologies also manufactures fab and hence, also opens an opportunity of setting up a wafer manufacturing plant in future. However, currently the plant will be limited to the OSAT business. The company's new facility will enable assembly and test manufacturing for both DRAM (Dynamic RAM) and NAND (NOT-AND) products and address demand from domestic and international markets. The phased construction of the new assembly and test facility in Gujarat is expected to begin in 2023F. Phase-1, which will include 500,000 sq.ft. of planned cleanroom space, to become operational in late 2024F, and Micron Technologies will ramp capacity gradually over time, in line with global demand trend. Micron Technologies expects Phase-2 of the project, which includes construction of a facility similar in scale to Phase-1, to start in the second-half of the decade. The company's investment will be up to US$825m over the two phases of the project. It will receive 50% fiscal support for the total project cost from the central government and incentives, representing 20% of the total project cost, from the Gujarat government. The combined investment by Micron Technologies and the two government entities over the course of both phases will be up to US$2.75bn. It must be noted that this is an entirely different industry compared to Kaynes Technology's business and will also include advanced packaging methodologies.

Figure 29: Although the market is dominated by wire-bonding, Micron Technologies has a healthy presence in TSV/WLCSP



SOURCE: INCRED RESEARCH, COMPANY REPORTS

Figure 30: Memory devices in high-end laptops require TSV packaging

Interconnection	Wire	Flip Chip	TSV	Hybrid³
Image				
Memory Application	DRAM (Mobile), NAND	DRAM (Computing, Graphics)	DRAM (HPC/Server, Graphics)	DRAM (HPC/Server, Graphics)
Number of I/Os	×4, ×8, ×16	×4, ×8, ×16	×1,024	×1,024
Number of Physical Interconnections	50-150 ea.	150-200 ea.	Bottom die: 5-8 K ea. Upper die: 3.5-10 K ea. (Up to 200 K ea. with dummy bumps)	Bottom die: 5-8 K ea. Upper die: 3.5-10 K ea. (Up to 200 K ea. with dummy bumps)
Interconnection Length	200 µm-2,000 µm	50 µm	20 µm	5 µm
Number of Stacks	2 / 4 / 6 / 8 (DRAM)	1 / 2 (Planar)	4 / 8 / 12	4 / 8 / 12 / 16
Max. Capacity / PKG	16 GB	4 GB	24 GB	32 GB

SOURCE: INCRED RESEARCH, COMPANY REPORTS

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